REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the application and amended Claims 11-15 in a previous response. In the present response, the Applicant has not amended, canceled or added any claims. Thus, Claims 1-20 are currently pending in the application.

Previously, the Examiner indicated that Claims 16-20 were allowed and that dependent Claims 2-5, 7-10 and 12-15 would be allowable if rewritten in independent form including all of the limitations of the base claims and intervening claims. In the present office action, the Examiner has rejected all of the pending claims. The Applicant respectfully disagrees as indicated by the below arguments.

I. Rejection of Claims 1, 5-6, 10-11 and 15 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 5-6, 10-11 and 15 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,766 to Nguyen. The Applicant respectfully disagrees.

The Applicant does not find, and the Examiner does not assert, where Nguyen discloses generating an event signal based upon a first clock rate as recited in independent Claims 1, 6 and 11. Instead, Nguyen relates to a data vector synchronizer which transfers data vectors from a first domain and a first clock rate to a second domain at a second clock rate for any frequency or phase relationship between the first clock rate and the second clock rate. (*See* column 1, lines 6-11.) Thus, Nguyen discloses transferring data from one time domain to another time domain but is silent on generating an event signal based upon a first clock rate.

Nevertheless, even assuming the data vector is an event signal, Nguyen does not teach synchronizing the data vector to the second clock domain based upon an edge transition of the data

vector and the second clock rate. Instead, the clock sync circuit in Nguyen captures the data vector input in holding registers at the 0 to 1 transition of a write-clock signal when an enable-write-clock signal is active. After deactivating the enable-write-clock signal, the clock sync circuit activates an enable-read-clock signal synchronously to a read-clock signal which causes sampling registers to capture the content of the data vector which in the holding registers at the 0 to 1 transition of the read-clock signal. (*See* column 6, lines 3-20.)

Thus, Nguyen discloses transferring the data from the first time domain to the second time domain based on the enable-read-clock signal being active and a transition of the read-clock signal. Nguyen does not consider an edge transition of the data vector. On the contrary, Nguyen ensures that the data is not changing before moving the data to the second time domain. (*See* column 3, lines 51-58.)

As such, for at least these reasons, Nguyen does not disclose each and every element of independent Claims 1, 6 and 11. Accordingly, Nguyen does not anticipate Claims 1, 6 and 11 and Claims dependent thereon. The Applicant, therefore, respectfully requests the Examiner to withdraw the §102(b) rejection with respect to Claims 1, 5-6, 10-11 and 15 and allow issuance thereof.

II. Rejection of Claims 2-4, 7-9 and 12-14 under 35 U.S.C. §103

The Examiner has rejected Claims 2-4, 7-9 and 12-14 under 35 U.S.C. §103(a) as being unpatentable over Nguyen in view of U.S. Patent No. 6,260,152 to Cole, *et al.* The Applicant respectfully disagrees.

As discussed above, Nguyen does not teach generating an event signal. On the contrary, Nguyen does not even suggest generating an event signal but instead is directed to transferring data from one time domain to a second time domain. Nevertheless, even assuming that the data is an event signal, Nguyen does not teach or suggest synchronizing the data to a second clock rate based upon an edge transition of the data and the second clock rate. As mentioned above, no consideration is given to an edge transition of the data. Thus, even if the data was an event signal, Nguyen does not teach or suggest synchronizing an event signal to a second clock rate based upon an edge transition of the event signal and the second clock rate as recited in independent Claims 1, 6 and 11.

Cole relates to synchronizing circuits and a digital circuit for synchronizing multiple signals in systems having multiple clock domains. (*See* column 1, lines 7-10.) Cole has not been cited to cure the above deficiencies of Nguyen but to teach the subject matter of the above identified dependent claims. Thus, the cited combination of Nguyen and Cole does not provide a *prima facie* case of obviousness of independent Claims 1, 6 and 11 and Claims dependent thereon. Dependent Claims 2-4, 7-9 and 12-14, therefore, are not unpatentable in view of the cited combination. The Applicant, therefore, respectfully requests the Examiner withdraw the §103(a) rejection of Claims 2-4, 7-9 and 12-14 and allow issuance thereof.

III. Rejection of Claims 16 and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 16 and 20 under 35 U.S.C. §103(a) as being unpatentable over Nguyen in view of U.S. Patent No. 6,594,327 to Radi. The Applicant respectfully disagrees.

As discussed above, Nguyen does not teach or suggest generating an event signal or synchronizing an event signal to a second clock rate based upon an edge transition of the event signal and the second clock rate as recited in independent Claims 1, 6 and 11 and also in independent Claim 16. The Examiner recognizes Nguyen also does not teach or suggest a fast pattern processor as recited in independent Claim 16 and cites Radi to cure this deficiency of Nguyen. The Applicant does not find, however, where Radi, teaches or suggests generating an event signal or synchronizing an event signal to a second clock rate based upon an edge transition of the event signal and the second clock rate. On the contrary, Radi discloses latching input data with its incoming input clock and, when the next incoming clock is edge-detected, feeding the latched data into another clock domain. (*See* column 5, lines 38-41.) Thus, even if the data is considered an event signal, Radi discloses interfacing the data between different time domains based on the edge-detection of a clock signal, not based upon an edge transition of the event signal and the second clock rate. As such, Radi does not cure the above deficiencies of Nguyen.

Thus, the cited combination of Nguyen and Radi does not provide a *prima facie* case of obviousness of independent Claim 16 and Claim 20 which depends thereon. Claims 16 and 20, therefore, are not unpatentable in view of the cited combination. The Applicant therefore respectfully requests the Examiner withdraw the §103(a) rejection of Claims 16 and 20 and allow issuance thereof.

IV. Rejection of Claims 17-19 under 35 U.S.C. §103

The Examiner has rejected Claims 17-19 under 35 U.S.C. §103(a) as being unpatentable over Nguyen in view of Radi and in further view of Cole. The Applicant respectfully disagrees. As

discussed above, Nguyen does not teach or suggest generating an event signal or synchronizing the event signal to the second clock rate based upon an edge transition of the event signal and the second clock rate. Cole and Radi have not been cited to cure this deficiency of Nguyen. The cited combination of Nguyen, Cole and Radi, therefore, does not provide a *prima facie* case of obviousness of independent Claim 16 and Claims dependent thereon. As such, the cited combination does not render Claims 17-19 unpatentable. The Applicant, therefore, respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 17-19 and allow issuance thereof.

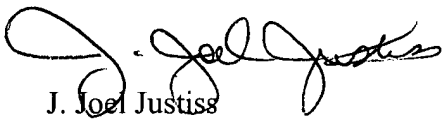
V. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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